ApplicationNOTE

GAMRY INSTRUMENTS

Testing Super-Capacitors
Part 1 – CV, EIS and Leakage Current

Introduction

Super-capacitors are energy storage devices similar to secondary batteries. Unlike batteries, which use chemical reactions to store energy, super-capacitors generally store energy through the physical separation of electrical charges.

All super-capacitors consist of two electrodes immersed in a conductive liquid or conductive polymer called the electrolyte. The electrodes are separated by an ionic-conducting separator that prevents shorts.

Compared to a battery, a super-capacitor has the following advantages:

- Higher charge and discharge rates (high power density)
- Longer cycle life (> 100,000 cycles)
- Low toxicity materials
- Operation over a wide temperature range
- Low cost per cycle

These are offset by some disadvantages:

- Higher self-discharge rate
- Lower energy density
- Lower cell voltage
- Poor voltage regulation
- High initial cost

Current applications for super-capacitors include:

- Hybrid Electric Vehicles (HEVs)
- Diesel engine starting systems
- Cordless power tools
- Emergency and safety systems

Many applications use a super-capacitor in parallel with a battery – a combination with a better cycle life and higher power than the battery alone.

For more information read Brian Conway's book on super-capacitor technology:

Conway, B.E., *Electrochemical Supercapacitors: Scientific Fundamentals and Technological Applications*, Kluwer Academic Press/ Plenum Publishers, NY, NY, 1999

Similar Technology, Confusing Names

A traditional Electrical Double Layer Capacitor (EDLC) uses electrostatic charge storage to store energy. Electrons in each electrode and ions in the electrolyte form a double layer capacitor. Typical capacitance of an electrochemical double layer is 20 $\mu F/cm^2$. Capacitance of micro-porous carbon with a surface area of 1000 m^2/gram can be as high as 200 F/gram.

Some devices, that we will call pseudo-capacitors, store charge via reversible Faradaic reactions on the surface of one or both electrodes. When electrode voltage is proportional to surface coverage and surface coverage is proportional to state-of-charge, these devices behave identically to capacitors. See Conway's book for details concerning these devices.

Unfortunately, technical papers and commercially available products have used many names for EDLCs and pseudo-capacitors. These include:

- Supercapacitors
- Ultracapacitors
- Aerogel capacitors
- Electrical double layer capacitors

Unless otherwise noted, this note will use the term super-capacitor for all high capacitance devices, regardless of charge storage mechanism.

Purpose of This Note

This application note is the first part of a two part overview of the electrochemical techniques used to test a super-capacitor device or technology. Part 1 discusses techniques familiar to electrochemists, while Part 2 discusses techniques familiar to battery technologists.

Commercial capacitors were tested to obtain results used in discussion of techniques.

The data in this note were recorded on a Gamry Instruments PWR800 system with optional EIS (EIS300) capability. All plots were generated using Gamry's Echem Analyst.

Item in yellow are specific to Gamry products.

Ideal Capacitor Characteristics

A capacitor is a storage device for electrical charge. The voltage of an ideal capacitor is proportional to the charge stored in the capacitor:

$$C\,V = Q$$

C is capacitance in Farads
V is voltage between the device's terminals (volts)
Q is the capacitor's charge in Coulombs (ampsec)

A capacitor's state-of-charge is easily measured - it is proportion to voltage. In contrast, measuring a battery's state-of-charge can be difficult.

The energy stored in a capacitor is:

$$E = \tfrac{1}{2}\,C\,V^2$$

E is the energy is Joules. Other terms were defined above.

The power drawn from a capacitor during discharge depends on the capacitor's voltage and the electrical current:

$$P = V\,I$$

P is power in watts.
V is the capacitor voltage in volts.
I is the discharge electrical current in amps.

An ideal capacitor loses no power or energy during charge or discharge, so the equation above can also be used to describe the charge process.

An ideal capacitor with no current flow will store energy and charge for ever.

Capacitor Non-ideality

The ideal capacitor does not exist – real capacitors have limitations and imperfections. The tests in this application note measure these limitations.

Voltage Limitations

The description of ideal capacitors did not mention voltage limitations. Capacitors can only operate within a "voltage window" with both an upper and lower voltage limit. Voltages outside the window can cause electrolyte decomposition damaging the device.

Capacitor electrolytes can be aqueous or non-aqueous. While aqueous electrolytes are generally safer and easier to use, capacitors with non-aqueous electrolytes can have a much wider voltage window.

When this was written, commercial single-cell super-capacitors have an upper voltage limit below 3.5 volts. High voltage devices have multiple cells in series.

Commercial super-capacitors are all uni-polar - the voltage on the plus (+) terminal must be more positive than the voltage on the minus (-) terminal. The lower voltage limit is therefore zero volts.

ESR

Real capacitors suffer power loss during charge and discharge. The loss is caused by resistance in the electrodes, contacts, and in the electrolyte. The industry standard term for this resistance is Equivalent Series Resistance (ESR). ESR is specified on the data sheet for most commercial capacitors.

One of the simplest models for a real capacitor is ESR in series with an ideal capacitor.

The power loss, P_{loss}, during charge or discharge is ESR times the current squared:

$$P_{loss} = I^2\ \ ESR$$

This power is lost as heat – under extreme conditions enough heat to damage the device.

Leakage Current

Leakage current is another capacitor non-ideality. An ideal capacitor will maintain constant voltage without current flow from an external circuit. Real capacitors require current, called leakage current, to maintain a constant voltage.

Leakage current can be modeled as a resistance in parallel with the capacitor. This model over simplifies the voltage and time dependence of leakage current.

Leakage current will discharge a charged capacitor that has no external connections to its terminals. This process is called self-discharge.

Note that a leakage current of 1 μA on a 1 F capacitor held at 2.5 V implies a 2.5 MΩ leakage resistance. The time constant for the self-discharge process on this capacitor is 2.5×10^6 seconds – nearly a month.

Time Effects

The time constant, τ, for charge or discharge of an ideal capacitor in series with ESR is:

$$\tau = ESR\ \ C$$

Typically, τ is between 0.1 and 20 seconds. A voltage step into a capacitor with ESR should create a current that exponentially decays toward zero. In a device with leakage current, the post-step current decay stops at the leakage current.

Commercial super-capacitors do not show this simple behavior. As seen below, commercial capacitors held at constant potential often take days to reach their specified leakage current. The time needed is much greater than predicted by τ.

One short-term time effect on a capacitor is a phenomenon electrical engineers call dielectric absorption. Dielectric absorption is caused by non-electrostatic charge storage mechanisms with very long time constants.

Time effects can be caused by slow Faradaic reactions occuring at imperfections on the surface of the electrode material. The carbon surfaces used for most super-capacitors have oxygen containing groups (hydroxyl, carbonyl…) that are plausible reaction sites.

Time effects could also be a side-effect of the porosity inherent in high capacity electrodes. Electrolyte resistance increases with distance into a pore. Different areas of the electrode surface therefore see different resistances. As discussed below, this complicates the simple capacitor plus ESR model into a distributed element or transmission line model.

Cycle life

An ideal capacitor can be charged and discharged for an infinite number of cycles. Many commercial super-capacitors approach this ideal - they are specified for 10^5 or even 10^6 charge/discharge cycles.

Secondary battery cycle-life specifications are typically hundreds of cycles.

The cycle life for all rechargeable devices depends on the exact conditions under which cycling occurs. Currents, voltage limits, device history, and temperature are all important.

Cyclic Voltammetry (CV)

Cyclic Voltammetry (CV) is a widely used electrochemical technique. Early in a capacitor development project, CV yields basic information about a capacitive electrochemical cell including:

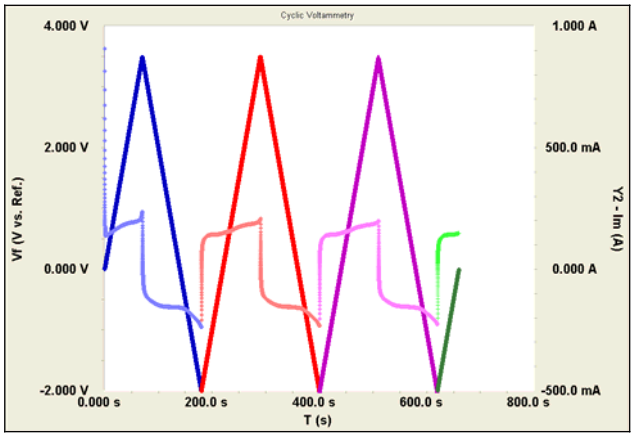
- Voltage window
- Capacitance
- Cycle life

A comprehensive description of CV is well beyond the scope of this document. Most books describing laboratory electrochemistry will have at least one chapter discussing CV.

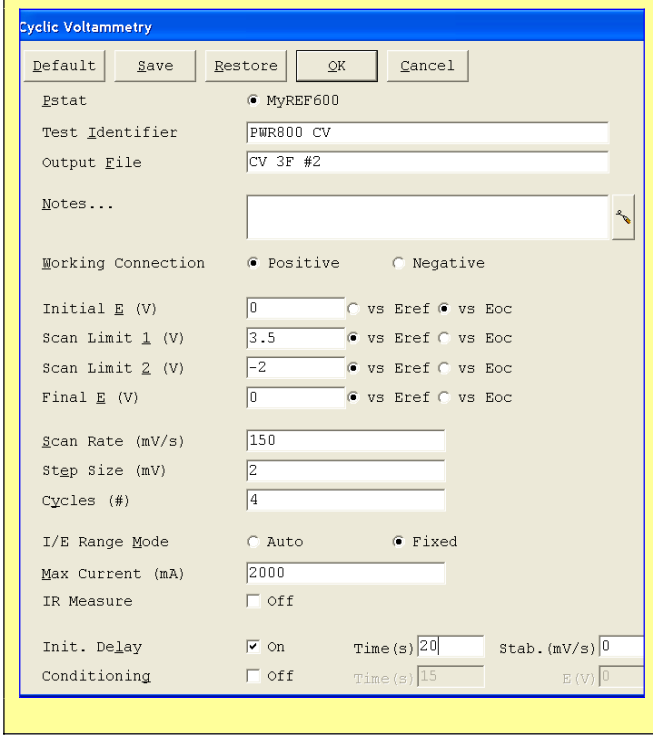
Description of CV

CV plots the current that flows through an electrochemical cell as the voltage is swept over a voltage range. A linear voltage ramp is used in the sweep. Often, a CV test will repetitively sweep the voltage between two limit potentials. A pair of sweeps in opposite directions is called a cycle.

The figure below displays a CV experiment as a plot of capacitor voltage and current versus time. The darker colored, saw-toothed waveforms are the voltage applied to the cell, the lighter colored waveforms are measured current. This graph shows a CV test with three and one-half cycles. Each cycle is shown in a different color.



The figure below shows Gamry's Setup for a CV test.



Four voltage parameters define Gamry's CV sweep range. The scan starts at the Initial E, ramps to Scan Limit 1, reverses and goes to Scan Limit 2. Additional cycles start and end at Scan Limit 2. The scan ends at the Final E.

CV can be run with two-electrode or three-electrode cell connections.

Three-electrode connections are common in fundamental research where they allow one electrode to be studied in isolation - without complications from the electrochemistry of the other electrodes. The three electrodes are:

- Working Electrode – the electrode being tested.
- Reference Electrode - an electrode with a constant electrochemical potential.

- Counter Electrode – generally an inert electrode present in the cell to complete the circuit.

Testing packaged capacitors requires two-electrode connections. All potentiostats can operate with two-electrode connections. Simply connect both the reference electrode and the counter electrode leads to one side of the capacitor. Connect the working electrode lead (and working sense lead if present) to the other side.

A voltage sweep applied to an ideal capacitor creates a current given by:

$$I = \frac{dQ}{dt} = C\frac{dV}{dt}$$

I is current in amperes

$\frac{dV}{dt}$ *is the scan rate of the voltage ramp*

Voltage scan rates for super-capacitor testing are usually between 0.1 mV/sec and 1 V/sec.

Scan rates at the lower end of this range allow slow processes to occur, but take a lot of testing time.

Fast scan often show lower capacitance than slower scans. This effect will be discussed below.

Be careful - fast scans on high value capacitors may require more current than the instrument can output or measure. The maximum allowed scan rate is:

$$\left(\frac{dV}{dT}\right)_{max} = \frac{I_{max}}{C}$$

I_{max} *is the instrument's maximum current in amperes*

Theoretical CV Plot

CV is plotted with current on the Y-axis and voltage on the X-Axis.

The next figure is a theoretical CV plot for a 3 F capacitor in series with a 50 mΩ ESR. The scan rate is 100 mV/sec. The scan limits were:

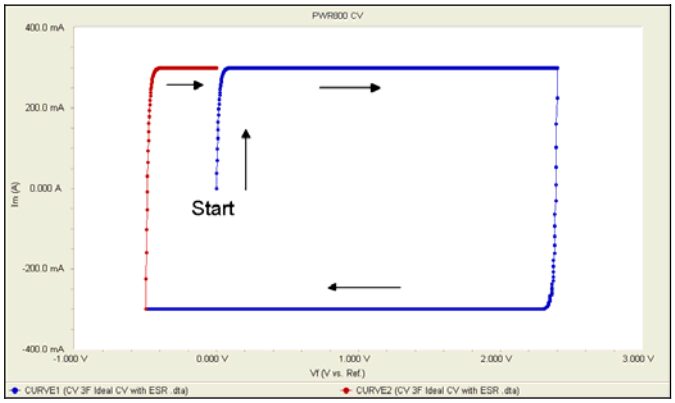
- Initial E 0.0 V
- Final E 0.0 V
- Scan Limit 1 2.4 V
- Scan Limit 2 -0.5 V

The scan's **Start** is shown on the plot along with arrows showing the direction of the scan. The second cycle is shown in red.

If this CV was recorded on an ideal capacitor (with no ESR), the CV plot would be a rectangle, with height:

$$I = C\frac{dV}{dt} = 300 \text{ mA}$$

ESR causes the slow rise in the current at the scan's start and rounds two corners of the rectangle. The time constant, τ discussed above, controls rounding of corners.



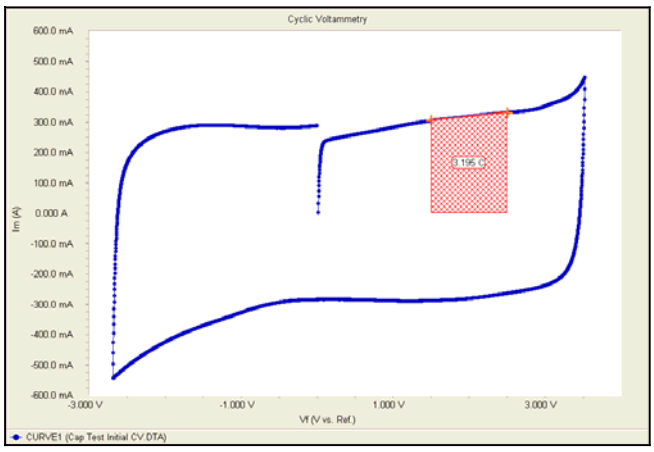
CV on a 3 F EDLC Capacitor

Most of this note's data were recorded using commercial 3 Farad EDLC capacitors. The parts tested were Nesscap P/N ESHSR-0003C0-002R7.

The 100 mV/sec cyclic voltammogram of a 3 F capacitor (below) illustrates how CV can determine a capacitor's voltage window. Notice this plot's similarity to the theoretical CV plot shown above.

The voltage limits entered in Setup were +5 and -3 volts. The scan was manually reversed when the current started to increase dramatically. The scan rate was slow enough that a user has time to react to the increased current. The reversal occurred at 3.5 volts – well beyond the 2.7 V specification for this capacitor. The negative going sweep was also manually reversed.

In Gamry's Framework, selecting **F2-Skip** reverses a sweep.



Integrating a segment of this curve shows calculation of capacitance from CV data. The integrated region (between 1.5 volt and 2.5 volts) is highlighted in red.

The integration range was selected using the Echem Analyst's **Select Range Using Keyboard** function.

Integration yielded the charge value shown on the curve. Capacitance is calculated from Q and the voltage range that was integrated:

$$C = \frac{Q}{\Delta V} = \frac{3.195\,C}{1\,V} = 3.195\,F$$

The calculated capacitance depends on the CV scan rate, the voltage region used in the integration, and a myriad of other variables.

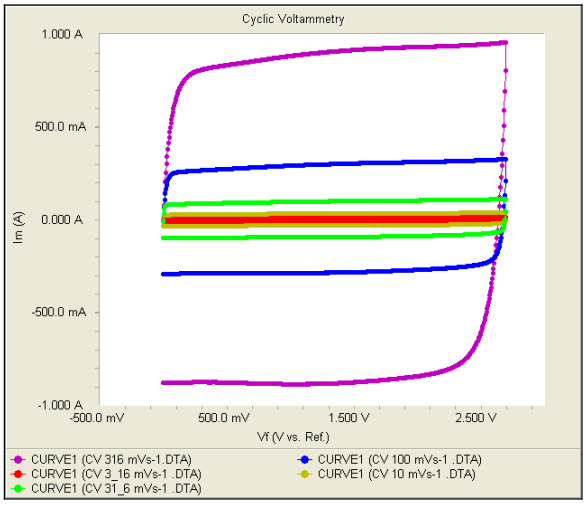
Important Note: Capacitor non-ideality precludes calculation of a true capacitance value for a real-world super-capacitor. Commercial super-capacitors have a specified capacitance value, valid when measured using a specific experiment. Other experimental techniques, including CV, EIS, and many long-term potentiostatic and galvanostatic tests, can give very different capacitance values.

CV Normalized by Scan Rate

A second capacitor was used to show CV's scan rate dependence. Voltammograms were recorded at scan rates of 3.16, 10, 31.6, 100, and 316 mV/sec. The capacitor was held at 0.0 volts for 10 minutes between scans. Scan limits were 0.0 and 2.7 volts.

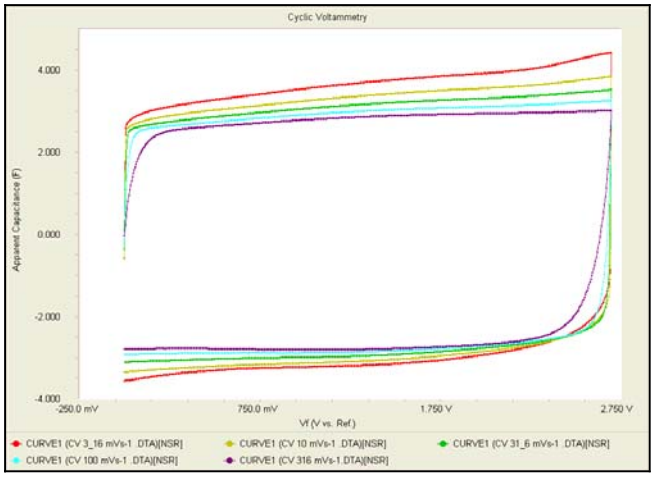
Note: Gamry's Sequence Wizard is a convenient tool for setting up complex experiments like this. The zero volt delay and a CV test were put inside a loop. The scan rate was multiplied by √10 between tests.

A plot of the data obtained from these scans is shown below: The purple curve was recorded at the highest scan rate and the red curve at the lowest scan rate.



The next figure shows these voltammograms normalized by dividing all currents by the scan rate.

Use the Echem Analyst's **CV, Normalize By Scan Rate to command to** normalize CV data. Select each curve in overlaid data using the Curve Selector before executing this command. Normalization creates a new curve with NSR in the curve's filename.



Scan rate normalized CV curves of an ideal capacitor superimpose – capacitance does not depend on scan rate. After normalization, the Y-axis units of ampsecvolt^{-1} become capacitance in Farads.

Super-capacitors are not ideal, so normalized plots do not superimpose. This note will call the Y-axis of a scan rate normalized CV apparent capacitance, C_{app}.

In the plot above, C_{app} is around 2.5 F on the curve with the highest scan rate (purple). This curve resembles the CV of an ideal capacitor plus ESR.

As scan rate decreases (blue, green, yellow, and red), the C_{app} rises and shows voltage dependence. This is expected for voltage driven chemical reactions.

C_{app}'s scan rate dependence can be explained by kinetically slow Faradaic reactions on the electrode surface and by transmission line behavior caused by electrode porosity. Both will cause an increase in C_{app} at lower scan rates.

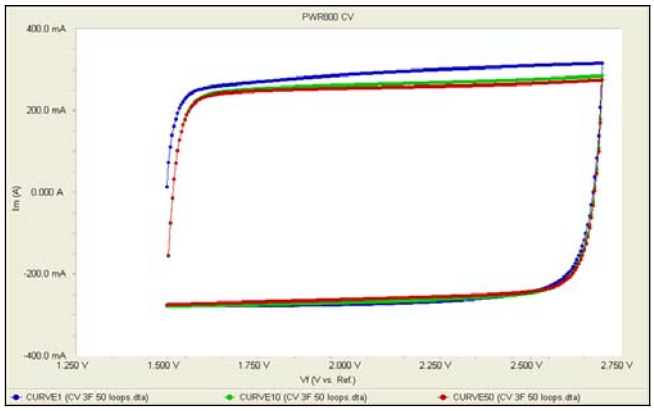
In the case where slow surface reactions are present, fast scans are over before the reactions occur – so all current is due to capacitance. Faradiac current has time to flow when scan rates are slower, increasing the total current and C_{app}.

A distributed element model will show similar scan rate behavior. Electrode surface that has high electrolyte resistance will not have time to respond to voltage changes during a fast scan. In effect, the fraction of electrode surface accessible to the electrolyte depends on the scan rate.

CV Used to Estimate Cycle Life

CV can also differentiate between poor cycle life and potentially useful cycle life.

The CV plot below shows 50 cycles between 1.0 and 2.7 volts, recorded using a 3 F capacitor. The 1st, 10th, and 50th cycles are shown in blue, green and red.

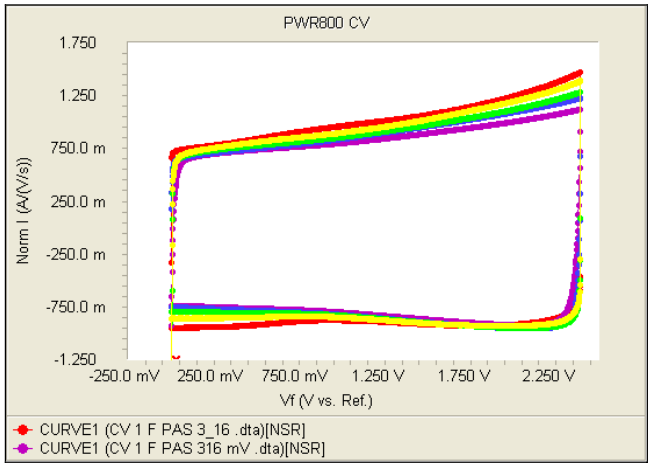


There is very little change in the data between the 10th and the 50th cycles. Therefore, this capacitor is worthy of cycle-life testing using cyclic charge-discharge techniques (described in Part 2 of this applications note).

CV on a Pseudo-capacitor

CV measurements on a pseudo-capacitor differ from the results measured on a true EDLC. We tested a 1 F PAS capacitor from Taiyo Yuden (part number PAS0815LR2R3105). The PAS acronym stands for Polyacenic Semiconductor which is a conductive polymer deposited on the electrodes.

CV tests were run on this device at 3.16, 10, 31.6, 100, and 316 mV/sec. The scan range was 0.0 to 2.4 V. The capacitor rested at 0.0 volts for 10 minutes between the scans.



The figure above shows the curves after normalization by scan rate. The red curve was recorded with the slowest scan rate and purple with the fastest. The Y-axis is apparent capacitance.

When compared to the normalized CV plot for the EDLC, one major difference is seen. The device's C_{app} depends on voltage at all scan rates. This is expected, given the Faradiaic nature of charge storage in this pseudo-capacitor.

EIS

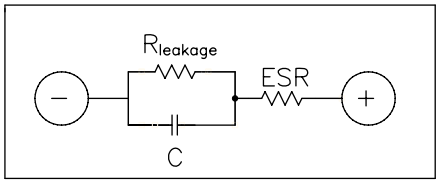
Electrochemical Impedance Spectroscopy (EIS) is the preferred method for measuring ESR of super-capacitors. It can also measure capacitance and measure capacitor non-ideality.

If you need basic information on EIS, see Gamry's Application Note at www.gamry.com:

Basics of Electrochemical Impedance Spectroscopy

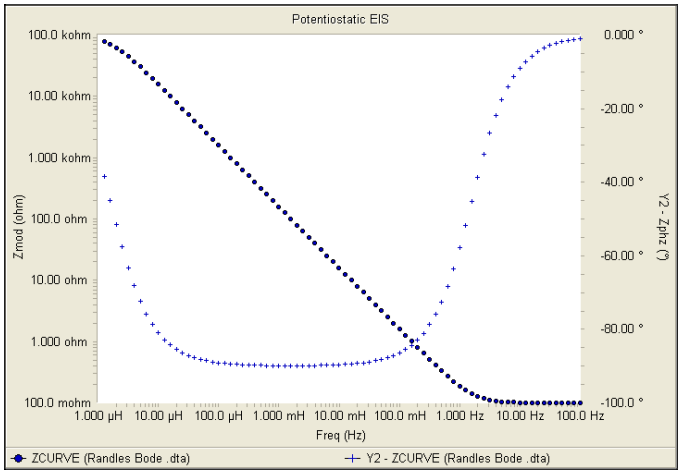
EIS Model for an Super-Capacitor

The most common model fitted to super-capacitor EIS spectra is a simplified Randle's model:



The elements in the model are:

C	- Ideal Capacitance
ESR	- Equivalent Series Resistance
$R_{leakage}$	- Leakage resistance



The EIS spectrum below is an ideal Bode plot of the Randle's model with:

- C 1F
- ESR 100 mΩ
- $R_{leakage}$ 100 kΩ

These values were chosen to approximate those of a typical EDLC device. The EIS magnitude is shown as circles and the phase is shown as crosses.

The Bode spectrum has three regions:

Above 10 Hz the magnitude and phase approach 100 mΩ and 0°. ESR dominates this region.

In the region between 100 μHz and 10 Hz, capacitance controls the impedance. Magnitude versus frequency is linear (on the log-log Bode plot) with a slope of -1 and the phase approaches -90°.

Below 10 μHz, the impedance begins a transition back towards resistive behavior as leakage resistance becomes dominant. This transition is incomplete, even at 1 μHz. EIS spectra of real devices rarely give much information about leakage resistance, because its effects are seen at impractically low frequencies.

EIS Measurement Mode

Gamry's EIS300 can measure EIS using three different control modes:

- Potentiostatic EIS
- Galvanostatic EIS
- Hybrid EIS

Potentiostatic and Galvanostatic modes control cell voltage and current respectively. Hybrid mode uses galvanostatic cell control, but changes the AC current to maintain a fixed AC voltage response.

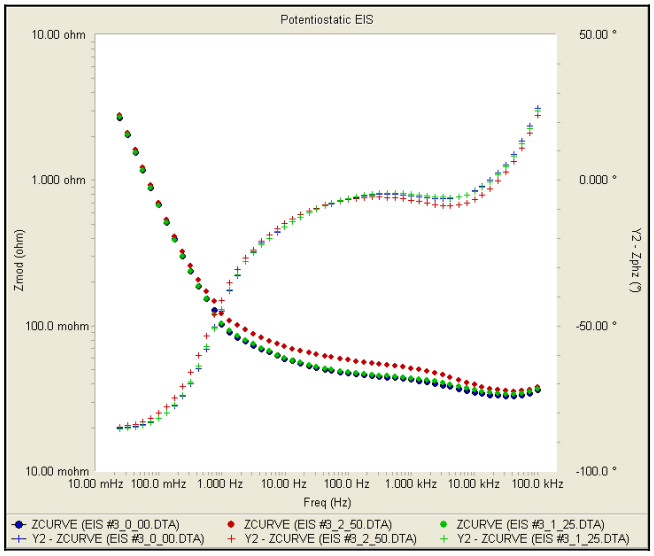
Galvanostatic and Hybrid mode EIS are preferred for very low impedance cells, where small errors in the DC voltage can create huge DC currents.

The impedance of the 3F capacitors used to generate data for this note is high enough that any control mode can be used. Potentiostatic mode is most common EIS mode, so this mode was used.

EIS Spectra on a 3 F EDLC at Different Potentials

The figure below is a Bode plot of EIS spectra of a 3 F EDLC recorded at three DC potentials: 0.0, 1.25 and 2.50 volts (in blue, green and red). The capacitor was held at the DC voltage for 10 minutes between spectrum acquisitions. The spectra were measured potentiostatically with an AC voltage of 1 mV_{rms}.

The Gamry Sequence Wizard was also used to record these data. The loop contained both an equilibration step and EIS data acquisition.



These spectra differ significantly from the ideal in the previous section. Differences include:

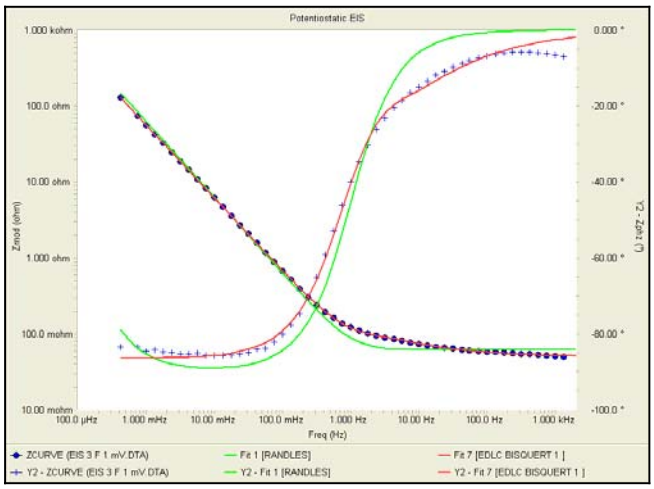
- No sign of the leakage resistance is seen in this frequency range.
- Phase between 1Hz and 100 Hz never approaches the simple model's 0° prediction.

The spectrum of an ideal capacitor is independent of DC voltage. Obviously, the EDLC characterized by these spectra shows non-ideality from 1 Hz to 10 kHz.

Fitting a Model to the Spectrum

The impedance spectrum below was measured on a 3 F EDLC potentiostated at 2.25 V.

Again, the data was recorded with a 1 mV excitation and potentiostatic cell control.

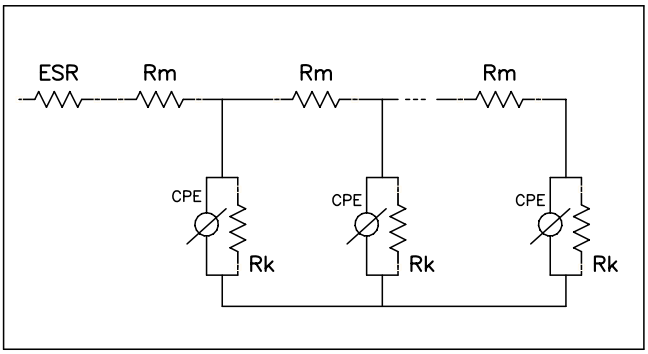


The green lines on this graph show a modified Randle's model fit to the data. The fit parameters are:

- C 2.51 F ± 12 mF
- ESR 62 mΩ ± 314 μΩ
- $R_{leakage}$ 773 Ω ± 59 Ω

The agreement between the Randle's model and the spectrum is poor. This is typical of EIS on EDLC capacitors where electrode porosity leads to very non-uniform electrolyte access to the electrode surface and Faradaic reactions occur. Simple resistor and capacitor models do not apply.

The fit to the data is much better using a porous electrode, transmission line model using a Bisquert open element is used. The model is:



The fit is seen in red on the Bode plot above. The fit parameters are:

- R_m 112 mΩ ± 22 mΩ
- R_k 2.2×10^{30} Ω ± 1×10^{38} Ω
- Y_m (CPE) 2.3 S•s/amp ± 0.15
- α (CPE) 0.960 ± 0.033
- ESR 50×10^{-3} Ω ± 639×10^{-6} Ω

For an explanation of the Model, see this application note at **www.gamry.com**:

Demystifying Transmissions Lines, What are They, Why are the Useful?

The high uncertainty in R_k is expected. The spectrum does not include frequencies where R_k affects the impedance.

EIS Spectrum of a Low ESR 650 F EDLC

EIS measurement on very low ESR capacitors is difficult. It generally requires:

- True 4-terminal measurements
- Galvanostatic cell control
- Low resistance contacts
- Twisted pair or coaxial cell leads

Two Gamry's Application Notes give suggestions for making low impedance EIS measurements:

Accuracy Contour Plots

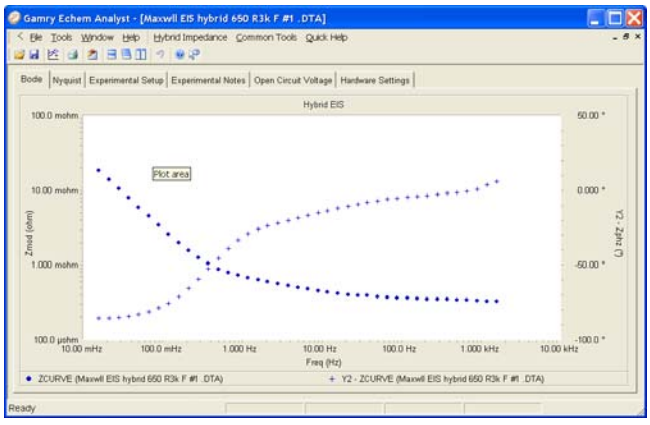
Verification of Low Impedance EIS Using a 1 mΩ Resistor

EIS spectra were recorded on a Maxwell capacitor (part number BCAP0650 P270). This 650 F capacitor was rated for ESR less than 600 μΩ at 1 kHz.

The photograph below shows the connections used to record the EIS spectrum of this device. 1.5 mm copper sheet was used to make the connections. Note that the current carrying leads and voltage sensing leads are on opposite sides of the device.

Caution: You need to be very careful to avoid shorting capacitor terminals though low resistance connections. Very dangerous currents of hundreds or even thousands of amps could flow.

The EIS spectrum is seen below. This spectrum was recorded in Hybrid Mode with a 1 mV AC voltage. Note that impedance at 1 kHz is 335 μΩ, which is less than this capacitor's rated ESR of 600 μΩ.

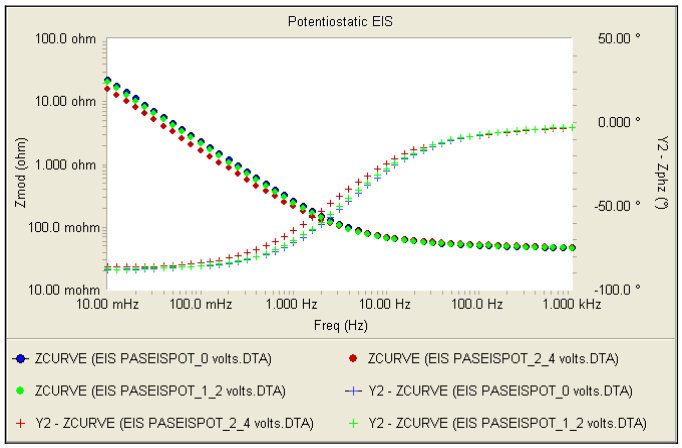


EIS on a Pseudo-Capacitor

EIS spectra recorded on an ideal capacitor at different DC voltages should superimpose.

EIS confirms the voltage dependence of measured capacitance on a PAS pseudo-capacitor. This is the same capacitor used previously for CV testing.

EIS spectra were recorded at DC voltages of 0, 1.2, and 2.4 V. Unlike the EDLC case, low frequency impedance was different at each voltage.



In the simple Randle's model, capacitance controls the impedance at the lowest frequencies in the graph above. In the plot above, impedance in this region depends on DC voltage, so the capacitance must also depend on DC voltage.

Leakage Current Measurement

Leakage current can be measured in at least two ways:

- Apply a DC voltage to a capacitor and measure the current required to maintain that voltage.
- Charge a capacitor to a fixed voltage, then open circuit the capacitor and measure the voltage change during self-discharge.

Conway's book includes a chapter that discusses leakage current and self-discharge of super-capacitors.

In an attempt to make the specifications of a super-capacitor look good, some manufacturers specify that leakage current is measured after 72 hours with voltage applied. Under these conditions, leakage current can be as low as 1 μA/F.

Direct Leakage Current Measurement

Direct potentiostatic measurement of capacitor leakage current is quite challenging. The test must apply a DC potential to capacitor being tested and measure extremely small currents.

Typically, capacitor charging currents are in amps and leakage currents are in microamps, a dynamic range of 10^6. Noise and/or drift in the DC potential can create currents that are larger than the leakage current.

For example, assume the 3 F capacitors used in our testing have an ESR of 100 mΩ. We want to measure a leakage current of 1 μA on these capacitors.

At frequencies where ESR is the dominant impedance, 0.1 μV of noise in the applied voltage will create a noise current of 1.0 μA. At lower frequencies, where capacitance dominates the impedance, a voltage drift of 0.3 μV/sec will create a current of 1.0 μA.

Fast data acquisition, external noise sources, or lack of a Faraday cage can lead to large apparent DC currents or continual switching between current ranges.

The Potentiostatic test in Gamry's PWR800 Electrochemical Energy Software will not accurately measure leakage current since it only offers a dynamic range of about 10^4.

The Chronoamperometry script in Gamry's PHE200 Physical Electrochemistry Software can measure μA currents on super-capacitors. The following experimental conditions are critical:

- Sampling mode must be set to Surface Mode.
- Sample period must be greater than 5 seconds.
- I/E Range mode must be set to auto.
- The test must be run in a Faraday cage to shield the sample from external noise sources.

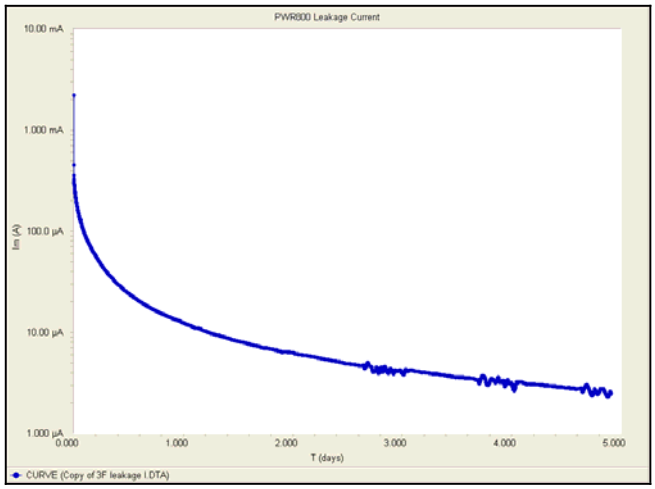
Surface mode is not available in the PHE200 Chronoamperometry technique before Revision 5.61 of the Gamry Framework.

PWR800 Leakage Current Measurement

The next figure shows leakage current measured on a new 3F capacitor. The plot is log current versus time for five days at 2.5 V.

Note that current is still falling five days after application of the potential. The manufacturer specifies leakage current on this capacitor at less than 5 μA after 72 hours – the measured value was about 3.2 μA.

The data in this plot was smoothed using a Savitsky-Golay algorithm with a 60 second window. The periodic noise signal is caused by daytime air conditioning.



Gamry does not want to force PWR800 users to buy Gamry's PHE200 Physical Electrochemistry software if they need to measure leakage current.

A special script has been developed for direct leakage current measurement using the PWR800 tools. This script, added to the PWR800 in Rev 5.61, is named:

PWRLeakageCurrent.exp

Unlike the PWR800 Potentiostatic technique, this script applies a voltage using the instrument's potentiostat mode and measures leakage current.

It uses a user entered estimate for ESR to avoid I/E Converter ranges where voltage noise can overload the current measurement circuitry. 10x gain in the current measurement allows measurement with 10x greater voltage noise and drift.

Measurement of Self-discharge

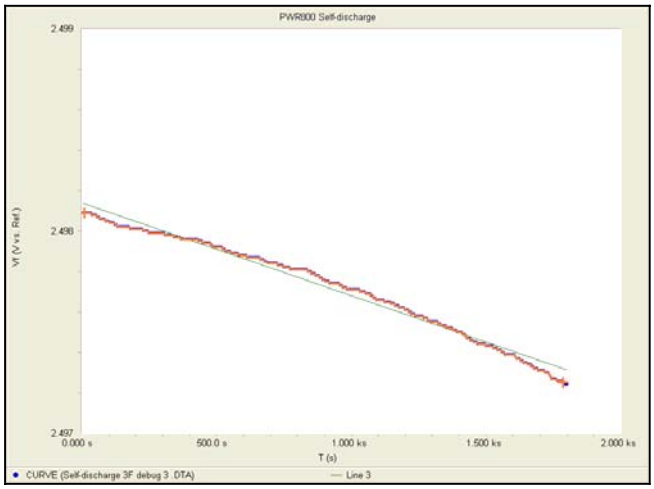
Self-discharge causes the open-circuit voltage of a charged capacitor to decrease over time. During self-discharge, leakage current discharges the capacitor - even though there is no external electrical current.

Conway's book describes three mechanisms for self-discharge. These mechanisms can be distinguished by analyzing the shapes in voltage versus time curves recorded over long time periods. This analysis was not done on the data presented here.

Instantaneous leakage current, I_{leak}, can be calculated by multiplying the rate of voltage change during self-discharge by capacitance.

$$I_{leak} = C\frac{dV}{dt}$$

The graph below is the open circuit voltage versus time curve of a 3 F capacitor open-circuited after 12 hours at 2.5 V. This was recorded with the capacitor pre-charged to 2.5 V in the previous test. The voltage change was less than 2 mV after 30 minutes.



The red line on the graph is a linear-least-squares fit of the voltage decay data. The slope is 0.55 µV/sec.

The leakage current is

$$I_{leak} = C \cdot \frac{dV}{dt} = 3\,\mathrm{F} \cdot 0.55\,\mu\mathrm{V/sec} = 1.6\,\mu\mathrm{A}$$

The slope calculation used the Linear Fit function in Gamry's Echem Analyst.

The PWR800 has added a script that makes this measurement. This script, added to Revision 5.61 of the PWR800 Software, is named:

PWR SelfDischarge.exp.

This script applies a constant potential for a user requested time. It then turns off the cell and measures changes in open circuit voltage. The instrument's offset and gain circuitry allows measurement of very small voltage differences.

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